PhD Qualifying Exam on Architecture
Fall 2004
Department of Computer Science
Georgia State University

NAME____

Question	*Score*
1	
2	
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total	

Note: You are only required to answer **six** questions out of the eight questions given below. **Do not** answer more than six questions. On the front page, put an X in the score area of the questions that you skip. On upper RIGHT corner of each answer sheet, write "Question # ___". On lower RIGHT corner of each answer sheet, write "Page # ___". Make sure pages are in order.

1. Refer to Figure 1. Make a truth-table for the signals in the circuit below (including Clock). Explain (in words) what is going on. Also explain how this circuit could be used.

Imagine that there was an inverter between signals a and b. How should the inverter be oriented? (that is, either signal b = a', or that signal a = b'). How and why would this improve the circuit? What would this truth table look like?

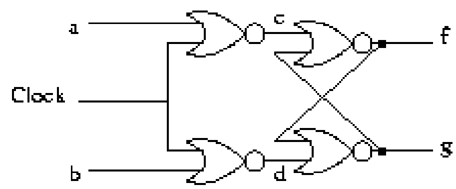

Figure 1.

2. The MOS Technologies 6510 is an 8-bit microprocessor with registers A, X, and Y. It allows commands like TAX, which can be decoded as "Transfer A's contents to X". Other commands include TXA, TAY, and TYA.

Using MUX's, registers, logic gates, etc., design a simple system that would implement the above commands, along with commands TXY and TYX. Also make a table showing what control values are needed to do these operations. Discuss your answer.

3. A memory system consists of a main memory of size 128k x 32 and a cache of 2K words. The cache uses direct mapping with a block size of 8 words.
a) How many bits are there in the tag, index, block, and word fields of the address format?
b) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.
c) How many blocks can the cache accommodate?

4. A computer responds to an interrupt request signal by pushing onto the stack the contents of PC and the current PSW (program status word). It then reads a new PSW from memory from a location given by an interrupt address symbolized by IAD. The first address of the service program is taken from memory at location IAD + 1.

a) List the sequence of microoperations for the interrupt cycle.
b) List the sequence of microoperations for the return from interrupt instruction.

5. Design an *n*-bit register *Q* using JK flip-flops that does the following. It has two input control signals, *S*1 and *S*0, that control the value loaded into bit *i* of the register *Q*. There

is also a second *n*-bit register, *A* that may provide input for register *Q*. The control signals have the following effect:

***S* 1**	***S* 0**	**Action**
0	0	Do nothing (i.e. bit *i* keeps its current value).
0	1	Make the value of bit *i* a 0.
1	0	Load bit *i* with the value of input *Ai*
1	1	Load bit *i* with the value (*Ai* XOR the current bit *i* value).

Design the circuit to implement the control signal actions.

6. The time delay of the four segments in the pipeline are as follows: t_1 = 50 ns; t_2 = 30 ns; t_3 = 95 ns; t_4 = 45 ns. The interface registers delay time t_r = 5 ns.

a.) How long would it take to add 500 pairs of numbers in the pipeline?
b.) How can we reduce the total time to about one-half of the time calculated in part (a)? Briefly explain your answer.

7. Assume that cache access time is t_c, cache block transfer time is t_b and hit ratio is h. Among blocks replaced in the data cache, P_d is the percentage of dirty blocks. Give the formulas for the effective access times for write-through, simple write-back, and flagged register write-back policies for the following two cases: (a) concurrent access to cache and memory and (b) sequential access to cache and memory.

8. Consider a five-stage adder/multiplier with a 10-ns delay per stage. Find the minimum number of periods required to perform the following operation (A1 * A2 * ... * A10) + (B1 * B2 * ... * B10) using this adder/multiplier pipeline. Here we assume that the pipeline can function either as an adder or a multiplier. We also assume that the output of stage 5 can be routed back to either of the two inputs X and Y of the pipeline with delays equal to a multiple of 10ns. Use figures to illustrate the details of your calculation.